CLAIMS

What is Claimed is:

1. A memory device comprising:

a first and a second port synchronization logic devices associated with a first and second port, respectively;

a port multiplexing logic; and

a single-ported memory core coupled to the port multiplexing logic, wherein the port synchronization logic devices synchronize information communicated between the first and second port associated with the port synchronization logic devices and the single-ported memory core by synchronizing information between port clocks and a core clock that is associated with the single-ported memory core.

2. A memory device as described in Claim 1 wherein the port multiplexing logic acts as a time division multiplexer (TDM) for the information communicated between the port synchronization logic devices and the single-ported memory core.

3. A memory device as described in Claim 1 wherein a bus for communicating between the port multiplexing logic and the single-ported memory core is at least twice the bandwidth of the highest of the port clocks.

4. A memory device as described in Claim 1 wherein the first port synchronization logic device comprises one or more FIFOs for synchronizing the information between a first port clock that is associated with the first port synchronization logic device and the core clock.

5. A memory device as described in Claim 4 at least part of the information is data from the single-ported memory core and wherein one of the FIFOs is a read data and control FIFO for synchronizing the data from the single-ported memory core.

6. A memory device as described in Claim 4 wherein at least part of the information is data, from the first port, that is to be written to the single-ported memory core and wherein one of the FIFOs is a write data and control FIFO for synchronizing the data from the first port.

7. A memory device as described in Claim 4 wherein at least part of the information is an address from the first port and wherein one of the FIFOs is an address FIFO for synchronizing the address from the first port.

8. A memory device as described in Claim 1 wherein the first port synchronization logic device further comprises one or more multiplexers used to bypass the synchronization of the information communicated between the ports and the single-ported memory core.

9. A memory device as described in Claim 8 wherein a write data and control FIFO is bypassed.

10. A memory device as described in Claim 8 wherein a read data and control FIFO is bypassed.

11. A memory device as described in Claim 8 wherein the port clocks and the core clock are all derived from a common clock generation circuit.

12. A dual ported memory device comprising:

a single port memory core operable at a first frequency;

a multiplexer logic coupled to said single port memory core;

a first port synchronizing logic coupled to a first port and coupled to said multiplexer logic; and

a second port synchronizing logic coupled to a second port and coupled to said multiplexer logic wherein said first and second synchronizing logic synchronizes information flow between said memory core and said first and second ports.

13. A dual ported memory device as described in Claim 12 wherein said first port is operable at a second frequency and wherein said second port is operable at a third frequency and wherein said second and third frequencies are independent.

14. A dual ported memory device wherein said first frequency is at least twice that of the fastest of the second and third frequencies.

15. A dual ported memory device as described in Claim 12 wherein said first port synchronizing logic comprises:

a read data and control FIFO circuit;

a write data and control FIFO circuit; and

an address FIFO circuit.

16. A dual ported memory device as described in Claim 15 wherein said second port synchronizing logic comprises:

a read data and control FIFO circuit;

a write data and control FIFO circuit; and

an address FIFO circuit.

17. A dual ported memory device as described in Claim 15 wherein said first port synchronizing logic comprises bypass logic for bypassing one of said FIFO circuits according to a configuration select line.

18. A dual ported memory device wherein said bypass logic is a multiplexer circuit.

19. A computer-usable medium having computer-readable program code embodied therein for causing a memory device to provide the functionality of a dual-ported memory using single-ported memory for multiple clocks, the method comprising:

receiving information at a first and second ports that are associated respectively with a first and second port synchronization logic devices;

communicating the information from the first and second ports, respectively, to the first and second port synchronization logic devices;

synchronizing the information, between the port clocks and a core clock associated with a single-ported memory core, at the first and the second port synchronization logic devices;

communicating the information from the first and second port synchronization logic devices to a port multiplexing logic that acts as a time division multiplexer (TDM) for the information; and

communicating the information from the TDM to the single-ported memory core.

20. A computer-usable medium as described in Claim 19, wherein a bus for communicating the information between the port multiplexing logic and the single-ported memory core is at least twice the bandwidth of the highest of the port clocks.

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